UNIVERSITY of GUELPH

COLLEGE of ENGINEERING AND PHYSICAL SCIENCES

SCHOOL OF COMPUTER SCIENCE

MSc Defence

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Graph Neural Networks for Circuit Clustering and Partitioning

Chair: Dr. Stacey Scott
Advisor: Dr. Gary Grewal
Co-Advisor: Dr. Shawki Areibi (SoE)
Non-Advisory: Dr. Luiza Antonie

Abstract:

Circuit clustering and circuit partitioning are essential tasks in the Very Large Scale Integration (VLSI) design flow and are usually solved using algorithmic techniques. Graph Neural Networks (GNNs), a branch of artificial neural networks, leverage the predictive power of deep learning on graph-structured data. Given the circuits' graphical nature, GNNs are increasingly applied to various VLSI design tasks.

This research investigates applying GNNs to solve circuit clustering and partitioning. Moreover, a hierarchical framework is suggested, linking the clustering GNN to the partitioning GNN, where information gained from clustering GNN enriches the initial dataset before being fed to the partitioning GNN. The proposed method motivates further exploration of preceding a clustering GNN to other GNNs addressing other VLSI layout design problems (e.g. placement), enhancing the node features. Furthermore, the proposed linkage between two distinct GNNs can be extended to other GNNs that solve consecutive tasks in VLSI system design.