UNIVERSITY of GUELPH

COLLEGE of ENGINEERING AND PHYSICAL SCIENCES

SCHOOL OF COMPUTER SCIENCE

MSc Seminar

Tuesday July 2, 2024, at 11AM, Reynolds 1101 (In-person)

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Graph Neural Networks for VLSI/FPGA Cad Flow Problems

Advisor: Dr. Gary Grewal
Advisory: Dr. Shawki Areibi (SoE)

Abstract:

This research explores the application of Graph Neural Networks (GNNs) to address circuit clustering and circuit partitioning, two essential tasks in Very Large Scale Integrated (VLSI) design. GNNs, a branch of artificial neural networks, leverage the predictive power of deep learning on graph-structured data. Due to the graphical nature of circuits, GNNs have seen increasing application in various VLSI design tasks.

In this research, we apply GNNs to circuit clustering and partitioning. We also propose a new hierarchical framework involving two consecutive GNNs: the first GNN does the clustering, and the second GNN does the partitioning. The information gained from clustering GNN is used to enrich the initial dataset. The second GNN uses this enhanced dataset for partitioning. This framework not only addresses the issue of insufficient initial node features but also highlights the highly connected areas for partitioning GNN. Additionally, the use of GNN for the clustering part aligns well with the partitioner and affects the depth of the overall model.