UNIVERSITY of GUELPH

COLLEGE of ENGINEERING AND PHYSICAL SCIENCES

SCHOOL OF COMPUTER SCIENCE

PhD Seminar 1

Tuesday October 12, 2021 at 1pm via Zoom

Timothy Martin

Integrating Machine Learning with FPGA Placement

Advisor: Dr. Gary Grewal
Co-Advisor: Dr. Shawki Areibi [Engineering]
Advisory: Dr. Luiza Antonie
Advisory: Dr. Radu Muresan [Engineering]

Abstract:

Placement and routing are two of the most challenging and time-consuming steps in the Field Programmable Gate Array (FPGA) computer-aided design flow. Recently Machine Learning (ML) methods have drawn the attention of researchers due to their effectiveness at reducing runtime and improving quality-of-result. In this seminar we propose three ML probes to help guide the FPGA placement process.
The first probe uses features available during early stages of placement to predict the routing congestion present in later placement iterations. Using this probe to guide the placer is shown to allow placer runtime to be reduced by up to 40% with no deterioration in quality-of-result.

Timing-driven placement relies on accurate delay estimates to correctly identify and optimize critical timing paths. The second probe uses features based on net characteristics, available routing resources, and the behaviour of the detailed router to predict interconnect delays during placement. Delays are predicted with over 94% accuracy and the critical path delay is reduced by 10% compared to a static delay model. It is imperative that the solution generated by the placer can be successfully routed. The third probe uses several simple ML models to predict whether a given placement is routable. We show that the routability of a placement can be correctly classified with over 97% accuracy.