



## COLLEGE of ENGINEERING AND PHYSICAL SCIENCES

SCHOOL OF COMPUTER SCIENCE

# PhD Seminar 2

**Thursday June 22, 2023 at 11am via Teams [Remote]**

**Timothy Martin**

*Integrating Machine Learning into the FPGA Design Flow*

**Advisor:** Dr. Gary Grewal

**Advisory:** Dr. Luiza Antonie

**Advisory:** Dr. Radu Muresan [Engineering]

### **Abstract:**

Placement and routing are two of the most challenging and time-consuming stages in the Field Programmable Gate Array (FPGA) design flow. In placement circuit components are assigned to physical locations on the FPGA hardware. Routing forms connections between components using the FPGA's network of wires and configurable switch boxes. As the FPGA market has grown, so too has the demand for increased performance on larger, more complex, devices. Existing computer-aided design tools for FPGAs struggle with the growing requirements, encountering long compile times and failure to achieve design closure. Recently, Machine Learning (ML) methods have drawn the attention of Electronic Design Automation (EDA) researchers for their ability to solve difficult problems more efficiently by taking a data-driven approach.

In this seminar, we examine three ways that ML can be used to improve the performance of placement and routing FPGA circuits. The first approach shows how ML probes can be developed to predict properties of the final routed solution during placement. Information is obtained about the solution quality, the demand on the FPGA architecture, and the expected routing difficulty.

With the second method we show how an ML controller can make a sequence of decisions to guide the placer. We demonstrate that different placement flows are better suited for different circuits and show how the ML controlled approach can outperform a static placement method.

In the third approach, we introduce a method for speeding up routing using both traditional ML and a deep-learning image-to-image model. The model forecasts the amount of congestion that each resource will experience during routing. Predictions are preloaded to the router prior to routing the circuit allowing it to make better decisions early on.